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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)

020254

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Application Number

10/083,684

Filed

February 27, 2002

First Named Inventor

Tomonari YAMAMOTO

Art Unit

2826

Examiner

Fazli ERDEM

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).

Note: No more than five (5) pages may be provided.

I am the

☐ applicant/inventor.☐ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)☐ attorney or agent of record.
Registration number _____☒ attorney or agent acting under 37 CFR 1.34. 56,171
Registration number if acting under 37 CFR 1.34 _____

Signature

Michael J. Caridi

Typed or printed name

202-822-1100

Telephone number

August 3, 2006

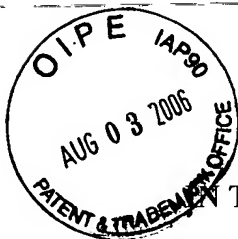
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.

☒ *Total of 1 forms are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **Tomonari YAMAMOTO et al.**

Group Art Unit: **2826**

Serial No.: **10/083,684**

Examiner: **Fazli Erdem**

Filed: **February 27, 2002**

Confirmation Number: **1544**

For: **SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD
THEREOF**

Attorney Docket Number: **020254**

Customer Number: **38834**

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop: AF

Commissioner for Patents

P. O. Box 1450

Alexandria, VA 22313-1450

Date: **August 3, 2006**

Sir:

This Request is filed concurrent with a Notice of Appeal in compliance with 37 C.F.R.

§41.31. Applicant requests review of the final rejection in the above-identified application.

No amendments are being filed with this request.

REMARKS

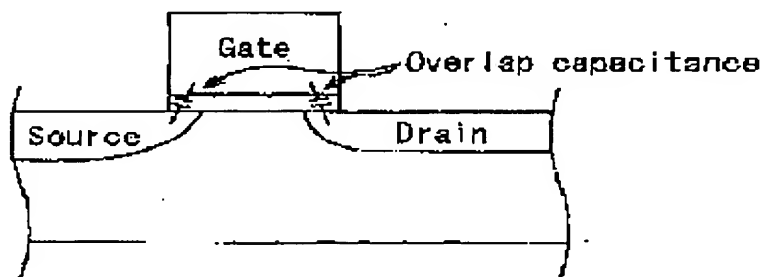
Claims 1-4, 6-10 12-14, 16-19, 21-23 and 25-32 are currently pending. Claims 1-4, 6-10 12-14, 16-19, 21-23, 25 and 26 are allowed.

Claims 27, 28 and 31 are rejected under 35 U.S.C. §103(a) as being unpatentable over **Talwar et al.** (U.S. Patent No. 6,380,044) in view of **Guegan** (U.S. Patent No. 5,705,410) further in view of **Esch** (U.S. Patent No. 4,056,825).

Claims 29, 30 and 32 are rejected under 35 U.S.C. §103(a) as being unpatentable over **Talwar et al.** (U.S. Patent No. 6,380,044) in view of **Guegan** (U.S. Patent No. 5,705,410) further in view of **Zhang** (U.S. Patent No. 6,855,954).

Claims 27 and 29 have a common limitation of an overlap capacitance between said gate and said source is $0.25 \text{ (fF/}\mu\text{m/side)}$ or more. The standing rejection of claim 27 relies on disclosures in **Esch** for the teaching of this limitation. See page 3, lines 4-6 of the May 5, 2006 Office Action. **Zhang** is relied upon for this limitation in the rejection of claim 29. See page 4, lines 1-4 of the May 5, 2006 Office Action. Applicants submit that there is clear error in maintaining that either **Esch** or **Zhang** teach or suggest this limitation.

The present application discloses that “the capacitance is an index showing the amount of overlap between the source and the drain and the gate electrode”, that is, a capacitance between the gate and the source indicates “an overlap capacitance.” See line 28 of page 36 to line 3 of page 37 of the specification. As in the reference drawing below, the overlap capacitance is a capacitance in the region where the gate electrode and the source (drain) overlap one another. The present application discloses that the amount of overlap between the source and the drain and the gate electrode is $0.25 \text{ (fF/}\mu\text{m/side)}$ or more.



Esch teaches a device wherein limiting the diffusion area 7' under a metal gate 15' and increasing gate oxide thickness reduces the parasitic capacitance. Specifically, the disclosure of column 5 is that the parasitic capacitance of the prior art illustrated in Fig. 5A is 0.034 pf-

per-mil along one side of the gate dimension over the diffused region. See col. 5, lines 8-22. This disclosure is contrasted to the invention of **Esch** which is illustrated in Fig. 5B and has a parasitic capacitance of 0.019 pf-per-mil. See col. 5, lines 32-37.

The Examiner appears to maintain that the skilled artisan would derive from this disclosure the motivation to utilize an overlap capacitance, as defined by the current application, of 0.25 (fF/ μ m/side) or more. Given the above described teachings of **Esch**, applicants respectfully submit that it is clear error to maintain that this limitation of claim 27 is set forth in the reference.

The present invention discloses and claims an index showing the sufficient amount of overlap capacitance in comparison with the conventional amount (0.20(fF/ μ m/side)). Wherefore, applicants respectfully submit that the limitation of claim 27 requiring an overlap capacitance between the gate and source of 0.25 (fF/ μ m/side) or more is not taught or suggested by the cited prior art.

In regard to claim 29, the Office Action specifically points to Figs. 5 and 6 and column 8 of **Zhang**. **Zhang** is directed to a thin film transistor and discloses two insulating films 10 and 11 formed over a gate electrode 4 and separating source 14 and drain 15 regions. Column 8 of **Zhang** discusses that these two insulating layers 10 and 11 have an overlapping parasitic capacitance of 1.04 fF between the gate and source sides. See col. 8, lines 3-29. The Office Action apparently asserts that based on this disclosure of **Zhang**, one of skill in the art would be motivated to achieve the claimed overlap capacitance of claim 29. However, there is no clear relation between the overlap capacitance of the currently claimed invention and the disclosure of Zhang.

As is well known, the case law surrounding 35 USC §103(a) requires that each limitation of the claimed invention be taught in the prior art, and that when a combination of references is made, there must be a teaching or motivation that suggests a reasonable likelihood of success in deriving the claimed invention. In the current instance, neither **Esch** nor **Zhang** teach the limitation of overlap capacitance as set forth in claims 27 and 29. Further, the teachings of **Esch** and **Zhang** as discussed above are completely removed from the currently claimed limitation of overlap capacitance. Therefore, there is no motivation or teaching to utilize the capacitance values set forth in these references in combination with the devices of **Talwar** and **Guegan**.

In view of the above remarks, Applicants submit that the rejection is improper. Accordingly, it is respectfully requested that the rejection of the claims be withdrawn and the application be passed on to allowance.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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